REMARKS

The specification has been amended to reflect that the document to be incorporated by reference is now a published patent application and to cite its publication and application numbers.

Claim 27 is rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter and in response, claim 27 is canceled.

Claims 1, 14 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Selvidge (U.S. Patent 6,009, 531). In response claims 1 and 14 are amended and claims 27-29 are canceled.

Claims 1, 14 and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Hyduke (U.S. Patent 7,003,746). In response claims 1 and 14 are amended and claims 27-29 are canceled.

Claims 2-13 and 16-26 are objected to as being dependant on rejected base claims. Base claims 1 and 14 are amended in response to this objection to render them patentable over the cited references.

The following comments distinguish claims 1 and 14 (as amended) over Selvidge and Hyduke.

A "primary" clock signal (which Selvidge calls "environmental clock signal" and which Hyduke calls a "user clock signal") is a clock input to an IC and its edges can indicate when a data signal input to the IC is valid. An IC will have more than one primary/environmental/user clock signal, for example, when its input signals are clocked differently. An IC normally includes "primitive" clock sinks (such as a latch or flip-flop) clocked by its primary clock signals for capturing the data conveyed by its data signals on each leading or trailing edge of a primary clock signal. Logic circuits within the IC process the data captured by the primitive clock sinks to produce the IC's output signals. An IC will also have synchronizing circuits that include clock sinks clocked by "secondary" clock signals the IC derives from its primary clock signals for capturing data transmitted between its internal logic circuits.

Referring, for example, to the applicant's FIG. 13, input clock sinks 12 clocked by a clock signal CLK1 provide data inputs to logic block 10 which processes the data to produce output signals captured by output clock sinks 14 to produce output signals (DATA_OUT) which could be IC output signals or which could be provided as inputs to other logic blocks within the IC. A clock logic circuit 63 derives a

secondary clock signal CLK2 from primary clock signal CLK1 that clocks output clock sinks 14.

Clock sinks 12 and 14 and clock logic 63 form a synchronizing circuit for synchronizing state changes in the captured DATA_IN and DATA_OUT data to edges of clock signals CLK1 and CLK2 that are derived from the IC's primary clock signals. The synchronizing circuit of FIG. 13 would be a "type B" synchronizing circuit if the two clock signals CLK1 and CLK2 are of the same domain, differing subdomain, and same phase.

The applicant's invention as recited in claim 1 relates to a method for programming a circuit emulator to emulate an IC described by a netlist. Since an emulator has difficulty emulating a type B synchronizing circuit, the applicants' method of claim 1 modifies the netlist to convert each type B synchronizing circuit into a type A synchronizing circuit in which the clock signals it employs to clock its input and output clock sinks are of the same domain, subdomain and phase. For example, the type B synchronizing circuit of FIG. 13 is converted into the type A synchronizing circuit of FIG. 16 in which its input and output sinks 12 and 14 are clocked by the same clock signal CLK1.

As recited in claim 1 (as amended) the clock signals that clock a synchronizing circuit's input and output sinks are all derived from at least one of the IC's primary clock signals both before and after its conversion from type A to type B. Note, for example, the CLK1 signal of FIG. 13, that clocks input sinks 12 and which is derived from a primary clock signal, continues to clock input sinks 12 of FIG. 16 and now also clocks output sinks 14.

Selvidge also teaches to transform synchronizing circuits described by a netlist before programming an emulator to eliminate clocking schemes that an emulator may not be able to emulate. For example, Selvidge's FIG. 3 shows a type B synchronizing circuit employing a logic circuit 126 an input clock sink 122 and an output clock sink. The Clk signal that clocks sink 112 is a primary (environmental/user) clock signal input to the IC, and the signal that clocks sink 124 is a secondary clock signal that logic circuit 114 is derived from Clk. Selvidge teaches to convert the synchronizing circuit of FIG. 3 to the type A circuit of FIG. 5A prior to emulation.

In FIG. 5A, the primary (environmental/user) clock signal Clk is no longer used to clock any clock sink, and no secondary clock signal derived from Clk is used to clock any clock sink. Instead, a new, higher frequency clock generated by a source VLCK within the emulator, and not derived from any of the IC's input primary (environmental/user) clock signals, now clocks clock sinks 122 and 124 (col. 7, lines 53-640). The transformed synchronizing circuit still makes use of the primary clock signal Clk, but not to clock any sinks. Instead a block of logic (Sync) converts the Clk signal into control signals Vgo provided as data inputs to new finite state machines 430 and 434 clocked by the high frequency VLKC signal which control enable inputs, rather than clock inputs, to clock sinks 122 and 124.

More generally, Selvidge teaches that regardless of how an IC derives the clock signals that clock its clock sinks from its primary (environmental/user) clock signals, the IC design should be modified to completely eliminate the use of any primary clock signals, or any secondary clock signals derived from them, for clocking any clock sinks. Selvidge teaches to revise all synchronizing circuits so that they all use the same system clock signal to clock their clock sinks (col. 10, lines 42-47), wherein the clock signal is generated by a source (VLCK) within the emulator and is not derived from any of the IC's primary (environmental/user) clock signals.

Hyduke teaches a generally similar approach to that of Selvidge, with one exception. Hyduke's FIG. 5 shows a primary (environmental/user) clock signal CLK clocking a clock sink 80 and a secondary clock signal (on line 97) derived from the CLK signal clocking another clock sink 81. Referring to FIG. 6, after a synchronizing circuit transformation, a main system clock signal (MSC) generated by the emulator and not derived from any of the IC's primary clock signals, now clocks clock sinks 80 and 81. Hyduke differs in one respect from Selvidge in that he recognizes that primary clock signals can always be used to clock primary clock sinks, such as clock sink 82 of FIG. 5 or 6, which receive the IC's input signals, and that it is therefore not necessary to modify a synchronizing circuit including primary clock sinks so that the primary clock sinks are clocked by the system clock signal MSC. (See col. 7, lines 35-43.)

Claim 1 as amended is patentable over Selvidge and Hyduke because it recites not only that a type B synchronizing circuit is converted into a type A synchronizing circuit, but that the resulting type A synchronizing circuit still derives all clock signals it uses to clock the input and output clock sinks "from the at least one primary clock signal provided as input to the IC ". Selvidge and Hyduke teach that when converting a type B synchronizing circuit to type A, the type A circuit is to clock its clock sinks with a system clock signal generated by the emulator that is not derived from any of the IC's primary input clock signals. Claims 1 and 14 are therefore patentable over Selvidge and Hyduke.

One advantage to the applicant's method is that by continuing to use clock signals derived from the IC's primary clock signals to clock all clock sinks after the synchronizing circuit conversion, it retains the same clock domains used by the IC originally described by the netlist, thereby rendering the clocking system of the emulated IC closer in nature to that of the IC described by the netlist. The applicant's approach type B to A synchronizing circuit conversions can also require fewer emulation resources to implement because the emulator need add only a multiplexer for each output sink (FIG. 16, devices 78), and need not add complicated state machines (Selvidge, FIG. 5A, devices 430, 434) or edge detectors (Hyduke, FIG. 6, device 102) for each clock sink, and because the applicant's conversion does not require the emulator to generate and route additional system clock signals (VCLK or MSC) to all synchronizing circuits as do Selvidge's and Hyduke's conversions. Finally, since the system clock Selvidge employs must run at a much higher frequency relative to user clocks, the simulation speed must be reduced in order to maintain the relationship. Thus, the applicant's approach permits the emulation to proceed more rapidly.

In view of the foregoing amendments and remarks, the application is believed in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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